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10/809,554	03/25/2004	Gary Dean Anderson	AUS920030980US1	7924

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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,554	ANDERSON ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20070706*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 5 objected to because of the following informalities:

Referring to claim 5, "the hardware affected" has no antecedent and is understood to refer to "the other hardware affected".

Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 10-14, 19 20 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Referring to claim 10, and subsequently claims 11-14, 19, 20, from paragraph 33 of the pre-grant publication, Applicant has indicated that such "computer readable medium" may comprise non-statutory subject matter. To overcome this rejection, Applicant must amend the claims to claim only storage media storing such instructions for execution.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6-13, 17-20 rejected under 35 U.S.C. 102(b) as being anticipated by US 6122756 to Baxter et al.

5. Referring to claim 6, Baxter discloses a computer system, having at least one processor, memory, and a bus coupled between the memory and the processor, comprising: a plurality of hardware units connected to the computer system by the bus (See figures 2-12);

a service processor having firmware (From line 1 of column 22, "As provided above, the EEPROMS 302 include the firmware for the microcontroller 300 and the JPs 250, particularly the JP designated as the diagnostic master and the microcontroller designated as the master microcontroller. The firmware for the microcontroller includes powerup testing, scan testing, error handling, system sniffing during run-time, and scanning error state when system fatal error occurs. The JP firmware includes powerup tests, XDIAG tests, manufacturing mode tests, and error handling.");

wherein when a first hardware unit of the plurality experiences an error, the first hardware unit is disconnected from the bus; and wherein the computer system is restarted without running a first diagnostic associated with the first hardware unit (From line 28 of column 16, "Such scanning is done when the system is powered up and also after the system detects a fatal error. The scanning operation includes automatically detecting a fault, automatically isolating the fault to at least a FRU and automatically de-configuring the system so as to logically and functionally removed the isolated

component/FRU. After the system is deconfigured, the system automatically re-boots itself and re-loads any applications program." From line 36 of column 24, "The master microcontroller runs the remaining off-board scan tests including power supply, blower, and backpanel interconnect testing. Any motherboards that were deconfigured as a result of previous testing will not be included in backpanel interconnect testing." Further, logically, if it is thusly disconnected it could not be tested.).

6. Referring to claim 7, 13, Baxter discloses the firmware of the service processor activates switches in circuitry of the computer system to disconnect the first hardware unit from the bus (From line 28 of column 16, "Such scanning is done when the system is powered up and also after the system detects a fatal error. The scanning operation includes automatically detecting a fault, automatically isolating the fault to at least a FRU and automatically de-configuring the system so as to logically and functionally removed the isolated component/FRU.").

7. Referring to claim 8, Baxter discloses a table is updated with information indicating the first hardware unit of the plurality has an error associated therewith (From line 14 of column 28, "Each Board Master collects all on-board information (e.g. which ASIC is good/bad, which JP is good/bad, its PROM revision number etc.) and writes it into NOVRAM.").

8. Referring to claim 9, 12, Baxter discloses a second hardware unit of the plurality that is affected by the error of the first hardware unit of the plurality is disconnected from the bus (From line 63 of column 6, "The computer system preferably operates so fault isolation is at least to the FRU which failed or to the FRU on which the component

believed to be faulted is located." From line 55 of column 21, "To deconfigure a JP daughter board 250, the CI ASIC 414 and the TLCC ASIC 408 mounted thereon is placed in HIGHZ mode. Alternatively, the JP 250 also can be placed in reset through a control register in the CI 414. To deconfigure a motherboard 202, all PI ASICs are placed in HIGHZ mode. Because the motherboard also has I/O devices on it, the I/O bus(ses) should be disabled via a control register in the GG ASIC 280." Further, logically, thusly deconfigured hardware comprises sub-hardware which is by extension deconfigured.).

9. Referring to claim 10, Baxter discloses a computer program product in a computer readable medium, comprising: a computer system having at least one processor, memory, a bus coupled between the memory and the processor, and a first hardware unit connected to the computer system; first instructions for detecting, by a service processor, when an error occurs associated with the first hardware unit of the computer system; second instructions for disconnecting the first hardware unit from a bus of the computer system; and fourth instructions for, when the computer system is rebooted, rebooting the computer system without running a first diagnostic associated with the first hardware unit (See figures 2-12. From line 1 of column 22, "As provided above, the EEPROMS 302 include the firmware for the microcontroller 300 and the JPs 250, particularly the JP designated as the diagnostic master and the microcontroller designated as the master microcontroller. The firmware for the microcontroller includes powerup testing, scan testing, error handling, system sniffing during run-time, and scanning error state when system fatal error occurs. The JP firmware includes powerup

tests, XDIAG tests, manufacturing mode tests, and error handling." From line 28 of column 16, "Such scanning is done when the system is powered up and also after the system detects a fatal error. The scanning operation includes automatically detecting a fault, automatically isolating the fault to at least a FRU and automatically de-configuring the system so as to logically and functionally removed the isolated component/FRU. After the system is deconfigured, the system automatically re-boots itself and re-loads any applications program." From line 36 of column 24, "The master microcontroller runs the remaining off-board scan tests including power supply, blower, and backpanel interconnect testing. Any motherboards that were deconfigured as a result of previous testing will not be included in backpanel interconnect testing." Further, logically, if it is thusly disconnected it could not be tested.); and

third instructions for indicating in a table entry in a second memory that the first hardware unit has an error associated therewith (From line 14 of column 28, "Each Board Master collects all on-board information (e.g. which ASIC is good/bad, which JP is good/bad, its PROM revision number etc.) and writes it into NOVRAM.").

10. Referring to claim 11, Baxter discloses the second instructions are firmware associated with a service processor of the computer system (From line 1 of column 22, "As provided above, the EEPROMS 302 include the firmware for the microcontroller 300 and the JPs 250, particularly the JP designated as the diagnostic master and the microcontroller designated as the master microcontroller. The firmware for the microcontroller includes powerup testing, scan testing, error handling, system sniffing during run-time, and scanning error state when system fatal error occurs. The JP

firmware includes powerup tests, XDIAG tests, manufacturing mode tests, and error handling.").

11. Referring to claim 17, 19, Baxter discloses the failed hardware is at least one bus interface unit, and wherein an error causing failure of the bus interface unit is a bus interface error (From line 7 of column 28 of Baxter, "JP runs extensive tests on the integrated SCSI and LAN controllers. These tests are run on each GG ASIC on a motherboard, one after another. If any of the tests failed, then that GG/PCI Bus subsystem will be deconfigured. Failure of both GG ASICs will cause the motherboard to be deconfigured.").

12. Referring to claim 18, 20, Baxter discloses responsive to the failed hardware no longer having the error, resuming operation by the failed hardware and other hardware associated with the failed hardware (From line 53 of column 2 of Baxter, "The computer system continues operation, albeit in a degraded condition, until the failed component is replaced/repaired by a service representative.").

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1, 2, 4, 5, 15, 16 rejected under 35 U.S.C. 103(a) as being unpatentable over US 6122756 to Baxter et al. in view of US 5774645 to Beaujard et al.

15. Referring to claim 1, Baxter discloses a method of processing errors in a computer system, having at least one processor, memory, and a bus coupled between the memory and the processor (See figures 2-12), comprising:

identifying, by a service processor (From line 23 of column 4, ""Diagnostic Master JP (DM)" shall be understood to mean the job processor/central processing unit in the system that coordinates all inter-board testing and in control when the system first halts into the main user interface."), failed hardware of the computer system (From line 24 of column 16, "The computer system 200 of the instant invention scans the boards, board mounted chips, busses, blowers and power supplies comprising the system to verify the integrity and operability of the system before applications are loaded.");

identifying, by the service processor, other hardware failed hardware within the computer system; deconfiguring the failed hardware and the other failed (From line 18 of column 26, "During the entire process of selecting a diagnostic master all failing tests and resulting motherboard/daughter board deconfigurations will be logged in each boards NOVRAM error log and the NOVRAM configuration tables. Just as had been done for the on-board microcontroller diagnostics and scan failures. At the completion of selecting the "diagnostic master", the diagnostic master JP will poll the various NOVRAMs to determine complete error and deconfiguration information, if any. All current system configuration information is now be written to the system ID SEEPROM

204."); and

rebooting the computer system without running a diagnostic on the failed hardware (From line 28 of column 16, "Such scanning is done when the system is powered up and also after the system detects a fatal error. The scanning operation includes automatically detecting a fault, automatically isolating the fault to at least a FRU and automatically de-configuring the system so as to logically and functionally removed the isolated component/FRU. After the system is deconfigured, the system automatically re-boots itself and re-loads any applications program." From line 36 of column 24, "The master microcontroller runs the remaining off-board scan tests including power supply, blower, and backpanel interconnect testing. Any motherboards that were deconfigured as a result of previous testing will not be included in backpanel interconnect testing." Further, logically, if it is thusly disconnected it could not be tested.).

Although Baxter does not specifically disclose that this other failed hardware is specifically identified as affected by the failed hardware, identifying such hardware is well known in the art. An example of this is shown by such concepts as root cause analysis, sympathetic errors, hierarchical analysis, etc... However, one specific example is shown by Beaujard, from line 50 of column 2, "Additionally, by grouping together cues, carried out when searching for a faulty element, the cues resulting directly or indirectly from a specified fault are ascertained, which cues need not therefore be taken into account during maintenance." A person of ordinary skill in the art at the time of the invention could have been motivated to identify such related failure because, as shown

in Beaujard, it saves time in maintenance, and further, Baxter has shown that such related errors are known, even if they are not explicitly indicated, and that while Baxter isolates as finely as it can, this may not be fine enough, from line 63 of column 6, "The computer system preferably operates so fault isolation is at least to the FRU which failed or to the FRU on which the component believed to be faulted is located."

16. Referring to claim 2, Baxter in view of Beaujard discloses the deconfiguring and rebooting steps are performed by the service processor (From line 23 of column 4 of Baxter, ""Diagnostic Master JP (DM)" shall be understood to mean the job processor/central processing unit in the system that coordinates all inter-board testing and in control when the system first halts into the main user interface.").

17. Referring to claim 4, Baxter in view of Beaujard discloses the step of deconfiguring includes activating at least one switch of circuitry of the computer system such that the failed hardware is excluded from the computer system (From line 28 of column 16 Baxter, "Such scanning is done when the system is powered up and also after the system detects a fatal error. The scanning operation includes automatically detecting a fault, automatically isolating the fault to at least a FRU and automatically de-configuring the system so as to logically and functionally removed the isolated component/FRU.").

18. Referring to claim 5, Baxter in view of Beaujard discloses the service processor identifies the failed hardware in a table entry in a second memory indicating that the failed hardware has an error, and wherein the hardware affected by the failed hardware is further identified in the table indicating it is associated with the failed hardware (From

line 14 of column 28 of Baxter, "Each Board Master collects all on-board information (e.g. which ASIC is good/bad, which JP is good/bad, its PROM revision number etc.) and writes it into NOVRAM.").

19. Referring to claim 15, Baxter in view of Beaujard discloses the failed hardware is at least one bus interface unit, and wherein an error causing failure of the bus interface unit is a bus interface error (From line 7 of column 28 of Baxter, "JP runs extensive tests on the integrated SCSI and LAN controllers. These tests are run on each GG ASIC on a motherboard, one after another. If any of the tests failed, then that GG/PCI Bus subsystem will be deconfigured. Failure of both GG ASICs will cause the motherboard to be deconfigured.").

20. Referring to claim 16, Baxter in view of Beaujard discloses responsive to the failed hardware no longer having the error, resuming operation by the failed hardware and other hardware associated with the failed hardware (From line 53 of column 2 of Baxter, "The computer system continues operation, albeit in a degraded condition, until the failed component is replaced/repaired by a service representative.").

21. Claim 14 rejected under 35 U.S.C. 103(a) as being unpatentable over US 6122756 to Baxter et al. as applied to claim 12 above, and further in view of US 5774645 to Beaujard et al.

22. Referring to claim 14, Baxter discloses identifying, by the service processor, other hardware failed hardware within the computer system; deconfiguring the failed hardware and the other failed (From line 18 of column 26, "During the entire process of selecting a diagnostic master all failing tests and resulting motherboard/daughter board

deconfigurations will be logged in each boards NOVRAM error log and the NOVRAM configuration tables. Just as had been done for the on-board microcontroller diagnostics and scan failures. At the completion of selecting the "diagnostic master", the diagnostic master JP will poll the various NOVRAMs to determine complete error and deconfiguration information, if any. All current system configuration information is now be written to the system ID SEEPROM 204.").

Although Baxter does not specifically disclose that this other failed hardware is specifically identified as affected by the failed hardware, identifying such hardware is well known in the art. An example of this is shown by such concepts as root cause analysis, sympathetic errors, hierarchical analysis, etc... However, one specific example is shown by Beaujard, from line 50 of column 2, "Additionally, by grouping together cues, carried out when searching for a faulty element, the cues resulting directly or indirectly from a specified fault are ascertained, which cues need not therefore be taken into account during maintenance." A person of ordinary skill in the art at the time of the invention could have been motivated to identify such related failure because, as shown in Beaujard, it saves time in maintenance, and further, Baxter has shown that such related errors are known, even if they are not explicitly indicated, and that while Baxter isolates as finely as it can, this may not be fine enough, from line 63 of column 6, "The computer system preferably operates so fault isolation is at least to the FRU which failed or to the FRU on which the component believed to be faulted is located."

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See notice of references cited. Examiner **strongly recommends** Applicant give close and careful consideration to the references cited herein, as the concept of deconfiguring failed components for reboot is recited in the references often.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gabriel L. Chu
Primary Examiner
Art Unit 2114

gc